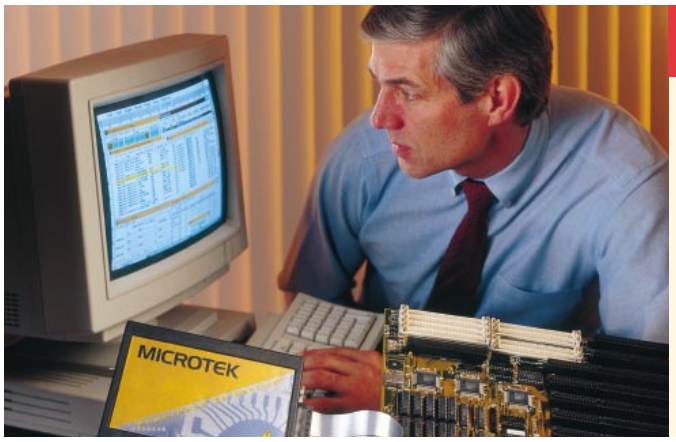

TECHNICAL DATA

MICROTEK

In-Circuit Emulators

for Intel486™ Processors

Helps You Solve Today's Most Difficult Software-Hardware Integration Problems

If you are an engineer designing embedded systems on an aggressive schedule, you will appreciate the practical features that make the PowerPack® 486 In-Circuit Emulator powerful and easy to use.

The full-featured PowerPack EA-486 In-Circuit Emulator integrates the capabilities of a powerful software debugger, the traditional features of an emulator, and the state analysis of a logic analyzer, all into one tool. The industry's most sophisticated trace and triggering system shows you details of your runtime system that are invisible with any other tool – like source code and related clock-edge hardware events of your real-time target system.

The new SWAT™ SoftWare Analysis Tool option now offers code coverage and performance analysis built into the emulator. The small probe size and flexible cables also make it easy to plug into the tightest embedded targets.

Three examples illustrate the debug power of the EA-486. Obviously there are many other examples that could be used and many more real world problems that the PowerPack family of emulators are capable of solving.

One of the most common problems that occurs during the integration stage of development is the "Ready Hang". It can occur for a number of reasons, one is when a reference is made to a memory location that does not actually have memory.

This problem frequently occurs because the software development environment that was used prior to hardware being available provided RAM at that location and the real target hardware does not. It can also be a symptom of an improperly dereferenced pointer that is pointing to the wrong address. The resulting situation is the processor stops processing, a situation commonly referred to as "Ready Hang". Since the RDY# never occurs, the processor never responds to commands and the development tool designed around the bond-out processor is also "hung". Normally the only way out of this situation is to reset the processor, which loses some of the important debug information.

Solution: The solution for the 486 processor is to setup a trigger that will count clock cycles within a bus cycle and provide a maximum count that would not be exceeded under normal conditions. If the maximum is exceeded the trace system automatically halts prior to the hang condition. . If the bus cycle completes before the count completes, the emulator will reset the trigger and start again. The 486 makes this a little tricky because there are two possible ready signals. The first is the normal RDY#, the other is the BRDY#, for Burst Ready. The best place to start counting clock cycles is when the Address has been qualified. Then you count until the Bus cycle complete signal is generated within the emulator. So you set up a trigger that begins the clock count when the Address becomes valid and counts 20 clocks or until the RDY# or the BRDY# occur.

Another type of debugging problem occurs when assessing the interrupt latency of a complex system.

Suppose when a hardware event occurs you have 600ns to begin the interrupt service routine. Here you have an event, which is a hardware request for interrupt services, and a problem of measuring time to actual service. The problem is providing a method to measure the time between the hardware event and the beginning of the service routine. This cannot be done by measuring bus cycles, since bus cycles have different numbers of clock cycles, you must measure the time absolutely.

Solution: The PowerPack EA-486 includes 8 independent triggers that monitor most address, data, control and status signals. External signals can also be monitored and included into the trace. These triggers are integrated with powerful counters and timers to allow easy real time detection of interrupt service latency that violates system requirements. In this case, set up a trigger such that when the hardware event signaling the inter-

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rupt occurs, the counter begins counting clock cycles. When you reach 20 clock cycles, you have 600ns (@33.3 MHz) and the emulator will halt (i.e. detect the 21st clock) if this is exceeded. If you get through the interrupt routine, you reset the trigger and immediately begin searching for the next violation.

Many integration problems can be solved faster with the extensive trigger capability of the EA-486.

An example of this might be the writing of a message buffer in a communications application. In this case there are ranges of allowable values for the data, which must be written into the buffer at certain locations. The idea is to halt the emulator if anything other than an allowable value is written into the buffer. Consider if the ranges of allowable values are the ranges (0 … 40), (100 … 140), and (200 … 240) within three address ranges. You would setup the triggers that qualify every write to the buffer and check for the given address and data range. If any of these or'd events were reached, the emulator will generate a trigger which can fource a breakpoint, or a number of other emulator actions.

Solution: There would be three events with address and data ranges as follows:

event1 = address range(1000:0000 to 1000:0255) NOT data (0 to 40)
event2 = address range(1000:0256 to 1000:0275) NOT data (100 to 140)
event3 = address range(1000:0276 to 1000:0300) NOT data (200 to 240)

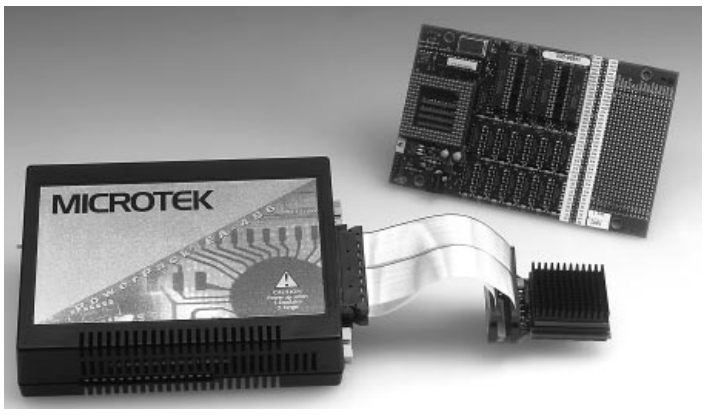
If you are within the address ranges of the communication buffer, but the data is NOT within the allowed data ranges, a breakpoint will occur. Even triggers of this level of sophistication only require 3 of the eight events available in the EA-486. These type of premium capabilities may seem unnecessary until you need them.

When the optional SWAT board is included, the PowerPack 486 provides code coverage and performance analysis in a single compact package using a single user interface without the need to instrument code. The PowerPack 486 tools provide the powerful features you need in a simple-to-use compact package.

PowerPack® EA-486

The EA-486 emulator provides full processor control features for debugging during development. It provides a view into the 486, showing the 486 based registers.

For the most demanding problems where hardware timing issues are affecting performance, incorrect memory reads and writes are affecting software operation, or you need to gather critical timing information on particular functions, the EA-486 provides 160-bit wide clock resolution trace to allow the engineer to track back and discover the problem. The user can view trace with clock cycle or bus cycle resolution or show only executed code, aligned with the data reads and writes that have occurred. A 40-bit time stamp is included to allow careful analysis of timing issues within portions of your code. The EA-486 trace includes qualifying hardware that allows the user to capture only the bus cycles of interest. This can be especially useful when debugging events that occur infrequently in the code.



To provide more in-depth software evaluation the EA-486 emulator can be outfitted with SoftWare Analysis Tools or SWAT. The SWAT option allows the user to evaluate his testing suite's code coverage down to the assembly code level. This can be a requirement in some mission critical environments. SWAT also provides performance analysis, showing time spent in particular modules, functions and even source statements. The results of the performance analysis can lead the developer to places where his code can benefit from optimization.

A key feature that is rarely considered until it is "too late" is the emulator's probe size. Probe insertion is a mechanical issue that can cause much extra work if the development tool is not flexible. Microtek's emulators provide a probe tip that is not much bigger than the processor itself. The probe tip connects to the emulator by flexible four inch cables. The result is a probe that is easy to install in most hardware targets. The overall small size of the emulator coupled with this probe tip and flexible cable make it easy to create simple fixtures to hold the emulator in place.

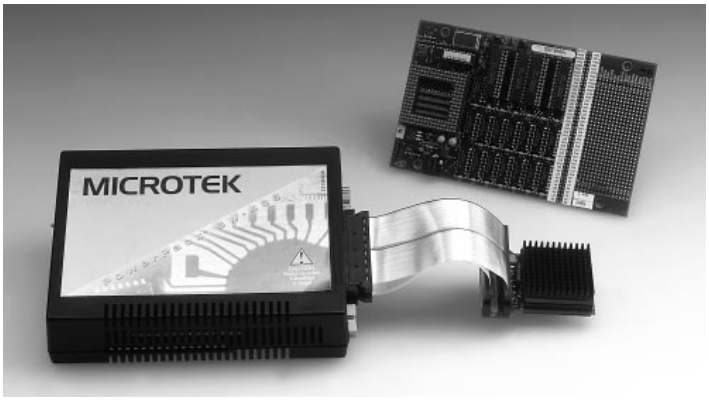
Confidence in the emulator is extremely important during product iterations. After many years of emulator design we have come to understand the necessity of a "gold standard" target available to check the development tool. When working with a target that is under constant revision the situation often arises where the emulator will not run the target as expected. The design engineer at this stage often questions whether the target, or the emulator has experienced a failure. To address this issue, Microtek developed a "Gold Standard" target system that ships with every EA emulator. The stand alone self test board (or SAST) coupled with

our built in test procedures check out the complete operation of the emulator. If the emulator is able to run our full suite of tests in the self test board, then the engineer has a very high degree of confidence that the emulator is functioning correctly. Using a self test board insures every functional block of the emulator is tested, including all of the control signals that interface to the target system.

System Features at a Glance:

- *Supports 33 MHz 486 processors*
- *Auto detects 3 volt or 5 volt operation*
- *Collects trace with clock edge resolution*
- *256k deep, 160 bit wide trace*
- *Trace records address, data, status and timestamp*
- *Timestamp using a 40-bit timer with a granularity of 40 ns.*
- *Qualified Trace allowing the trigger system to specify which microprocessor cycles will be captured*
- *Supports real, virtual-86, protected and system management modes of the processor*
- *Source Level Debug for toolchains that produce OMF-386 output*
- *256 Software Breakpoints*
- *Triggers allow the user to specify up to eight independent complex events.*
- *Execution Breakpoints implemented using the 486 debug registers*
- *Ability to single step at the source or assembly level*
- *Trigger In/Out for cross triggering with other instrumentation*
- *View and edit internal registers*
- *Detailed self-test diagnostics with self-test hardware*
- *State-of-the-art design provides very low target signal loading*
- *Overlay memory available in 1 megabyte or 4 megabyte size*

PowerPack® SW *Plus* 486



Microtek understands that not all projects require the extensive features of the EA-class of emulators. For projects with a tight budget, the SW *Plus* class of emulators is the perfect choice.

Just like the EA-class emulator it provides a view into the 486 based registers. Important processor control features are supported including: software breakpoints, execution breakpoints, single stepping, stepping through function calls, and breaking on memory writes to data space or memory access to I/O space. For more difficult problems where software is losing control of the processor, or unexpected error routines are being called, the emulator provides full bus level and instruction trace to allow the engineer to track back and discover the problem. The SW *Plus* 486 emulator can also be enhanced with the SWAT option, providing critical code coverage and software performance information.

System Features at a Glance:

- *Supports 33 MHz 486 processors*
- *Auto detects 3 volt or 5 volt operation*
- *Displays trace with bus cycle resolution*
- *128k deep, 160 bit wide trace*
- *Trace records address, data, status and timestamp*
- *Timestamp using a 40-bit timer with a granularity of 40 Ns.*
- *Qualified Trace allowing the trigger system to specify which microprocessor cycles will be captured*
- *Supports real, virtual-86, protected and system management modes of the processor*
- *Source Level Debug for toolchains that produce OMF-386 or OMF-86 output*
- *256 Software Breakpoints*
- *Triggers allow the user to specify up to eight independent complex events.*
- *Execution Breakpoints implemented using the 486 debug registers*
- *Ability to single step at the source or assembly level*
- *Trigger In/Out for cross triggering with other instrumentation*
- *View and edit internal registers*
- *Detailed self-test diagnostics with self-test hardware*
- *State-of-the-art design provides very low target signal loading*
- *Overlay memory available in 1 megabyte or 4 megabyte size*

T E C H N I C A L D A T A

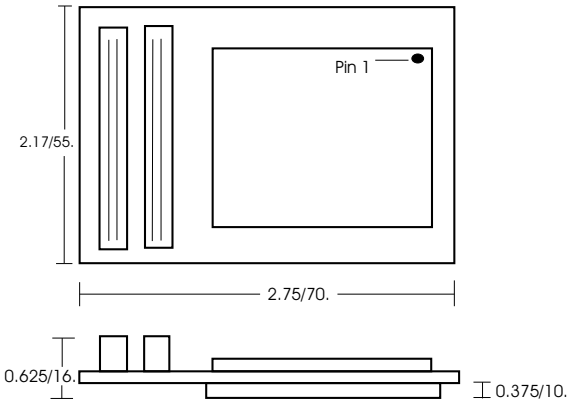
PC Host Requirements

PowerPack SLD requires a 486 or better PC (Pentium recommended) with a minimum of 8 megabytes of RAM (16 recommended for Win95), an SVGA or better color monitor, 3.5” floppy drive, a free serial port and a mouse.

Electrical Input . . . . . 100-120 VAC, 200-240VAC, 47-63 Hz
Consumption . . . . . 50W (max), 25W (typ)

Environmental

Operating Temperature . . . . . 10 to 35˚ C
Storage Temperature . . . . . 10 to 50˚ C
Relative Humidity . . . . . 20 to 80%
Shipping Weight . . . . . 8 lbs.



Probe Dimensions for SW/EA 386EX Emulator

EA-486 Adapters

The EA/SW-486 probe includes a 168-pin PGA male header. An adapter is required to connect to other package styles.

168-pin PGA to 196-pin PQFP clip-over adapter (clips over soldered-in 196-pin part) ET # is AC-PGA10-QF15-486 . . . . . 168PGA-196CO
168-pin PGA to 196-pin PQFP clip-over adapter (solders to target in place of 196-pin PQFP part) ET # AS-PGA10-QF15S-486 . . . . . 168PGA-196SD
168-pin PGA to 176 TQFP clip-over adapter (clips over 176-pin SX processor) ET # is AC-PGA10-QF67-486SX 168PGA-176SXCO
168-pin PGA to 176 TQFP solder-down adapter (solders to target in place of 176-pin SX processor) ET # AS-PGA10-QF67S-486 . . . . . 168PGA-176XSD
168-pin PGA to 176 TQFP clip-over adapter (clips over 176-pin GX processor) ET # is AC-PGA10-QF67-486GX 168PGA-176GXCO
168-pin PGA to 176 TQFP solder-down adapter (solders to target in place of 176-pin GX processor) ET # AS-PGA10-QF67S-486GX 168PGA-176GXSD
168-pin PGA to 208-pin SQFP clip-over adapter (clips over soldered-in 208-pin SWFP part) ET # is AC-PGA10-QF21-80486SL 168PGA-208C
168-pin PGA to 208-pin solder-down adapter (solders to target in place of 208-pin SWFP processor) ET # AS-PGA10-QF21S-80486SL . . 168PGA-208SD

PRODUCT CODE	DESCRIPTION	
PP-EA 486DX/DX2	**PowerPack EA-486**	PowerPack EA-486 emulator, 33 MHz, SAST, 256K trace, no overlay
PP-SW Plus 486DX/DX2	**PowerPack SW *Plus* 486**	PowerPack SW Plus 486 emulator, 25MHz, no trace, no overlay
PP-DX2-DX4	**DX4 probe head DX-DX4**	Probe head for supporting split voltage DX4 and GX processors
PP-OVM-1MEG	**Overlay Memory Module**	Zero wait state overlay memory module, 1 megabyte
PP-SWAT486-1MEG	**Software Performance**	Software performance analysis option with 1Megabyte
PP-SWAT486-4MEG	**Software Performance**	Software performance analysis option with 4 Megabytes
PP-486-SAST	**Self test board**	Stand-alone self-test board

Products are warranted against defects in materials or workmanship for a period of 90 days. Contact your sales representative for information on our Gold Support Program – this provides hardware, software, and firmware updates, plus repair coverage for your emulator.

For more information about Service Support Options to match your project requirements, contact Lisa Rice at (800)886-7333x4038.

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